What is claimed is:

1. A semiconductor device having an etch stopper formed of a nitride film using low temperature atomic layer deposition, the semiconductor device comprising:

a gate pattern which is formed on the semiconductor device and comprises a top layer formed of a first nitride film using low pressure chemical vapor deposition and a gate spacer;

an etch stopper which covers the semiconductor substrate and the gate pattern and comprises a second nitride film formed using low temperature atomic layer deposition; and

an interlayer insulating film which is formed on the etch stopper.

2. The semiconductor device of claim 1, wherein the gate pattern of the semiconductor device comprises:

a gate electrode which is formed on the semiconductor substrate and comprises polysilicon; and

a silicide layer formed on the gate electrode; wherein

the top layer is formed on the silicide layer and comprises the first nitride film formed using low pressure chemical vapor deposition; and

the gate spacer is formed on the sidewalls of the gate electrode, the silicide layer, and the top layer and comprises the first nitride film formed using low pressure chemical vapor deposition.

3. The semiconductor device of claim 1, wherein the etch stopper is formed at a temperature of 100 to 500°C.

4. The semiconductor device of claim 1, wherein the thickness of the etch stopper is within 100 to 700Å .

5. The semiconductor device of claim 1, wherein the interlayer insulating film

is a single film formed of an oxide film including one of SiO_2, BPSG, HDP oxide, and Fox.

6. The semiconductor device of claim 1, wherein the interlayer insulating film is a multi-layer film including films comprising an oxide film including one of SiO_2, BPSG, HDP oxide, Fox.

7. A method for fabricating a semiconductor device having an etch stopper formed of a nitride film using low temperature atomic layer deposition, the method comprising:

forming a gate pattern on a semiconductor substrate in which the gate pattern includes a first nitride film formed using low pressure chemical vapor deposition for a top layer and sidewalls;

forming an etch stopper which covers the gate pattern and the semiconductor substrate to a predetermined thickness and comprises a second nitride film formed using low temperature atomic layer deposition;

depositing an interlayer insulating film on the semiconductor substrate where the etch stopper is formed;

forming a self-aligned contact hole by dry etching the interlayer insulating film using the gate pattern as a mask; and

removing the etch stopper which is exposed to the self-aligned contact hole by wet etching.

8. The method of claim 7, wherein forming the gate pattern comprises:

depositing a gate electrode, a silicide layer, and a top layer, which comprises the first nitride film formed using low pressure chemical vapor deposition, on the semiconductor substrate;

etching the gate electrode, the silicide layer, and the top layer; and

forming the gate spacer, which comprises the first nitride film formed using low pressure chemical vapor deposition, on the sidewalls of the gate electrode, the silicide layer, and the top layer.

9. The method of claim 7, wherein the second nitride film formed by atomic layer deposition is formed at a temperature of 100 to 500°C.

10. The method of claim 7, wherein as a reaction gas for forming the etch stopper, one of SiH_4, $SiCl_2H_2$, and $SiCl_4$ is used as a silicon source, and one of N_2, NH_3, and N_2O is used as a nitrogen source.

11. The method of claim 7, wherein the thickness of the second nitride film is within 100 to 700Å .

12. The method of claim 7, wherein the interlayer insulating film is a single layer film formed of an oxide film including SiO_2, BPSG, HDP oxide, Fox.

13. The method of claim 7, wherein the interlayer insulating film is a multi-layer film including films comprising an oxide film including SiO_2, BPSG, HDP oxide, Fox.

14. The method of claim 7, wherein the dry etching for forming the self-aligned contact hole continues until the etch stopper is exposed.

15. The method of claim 7, wherein a hydrofluoric acid solution as an etching solution is used in the wet etching for removing the etch stopper.

16. The method of claim 7, wherein the wet etching for removing the etch stopper employs a SC1 cleaning method.